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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
YEUNG LOPEZ, FEIFEI	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,454	KNUDSEN, CARL	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _07 January 2008_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-22_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-22_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-11,13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kommerling et al (PG Pub 2001/0033012 A1), in view of Anthony et al (US Patent 6,404,674 B1), further in view of Minakata et al (PG Pub 2001/0005011 A1), and still further in view of “Self-Destructing Diskette” IBM Technical Disclosure Bulletin 33 (June 1, 1990): 218-219.

4. Regarding claim 1, Kommerling teach that an integrated circuit arrangement that is susceptible to data corruption caused by a local magnetic field, the integrated circuit arrangement comprising: an integrated circuit (fig. 1A); a data-storage arrangement

(memory 110 in fig. 1A); and an integrated circuit package (encapsulant 50 in fig. 1A) enclosing the integrated circuit and including a magnetic device (element 365 in fig. 5A) adapted to generate a local magnetic field, and the logic state of at least one of the magnetic states of information stored in a data storage is altered in response to a portion of the magnetic device being removed. Note in paragraphs [0026] and [0116], Kommerling teach that once tampering is detected, the secure content will be erased. Also note that erasing a secure content of a magnetic memory is altering the logic state of the magnetic memory. However, Kommerling do not teach that the magnetic memory being a plurality of mini magnets adapted to store logic states in response to electrical control signals, nor do Kommerling teach that the magnetic field is sufficiently strong to alter the logic state of at least one of the mini magnets. In the same field of endeavor, Anthony teach using a plurality of mini magnets to store logic states in response to electrical control signals (fig. 7, magnets 11). Furthermore, Minakata teach that a magnetic memory can be made highly integrated (paragraph [0044]), and therefore a small magnetic memory circuit can be achieved. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a plurality of mini magnets to store logic states in response to electrical control signals for the benefit of achieving a small magnetic memory circuit. Also, in the same field of endeavor, IBM teaches erasing sensitive information using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the

magnetic field generated by the magnetic device (element 365) of Kommerling sufficiently strong to alter the logic state of the data storage for the benefit of providing a tamper-proof storage medium.

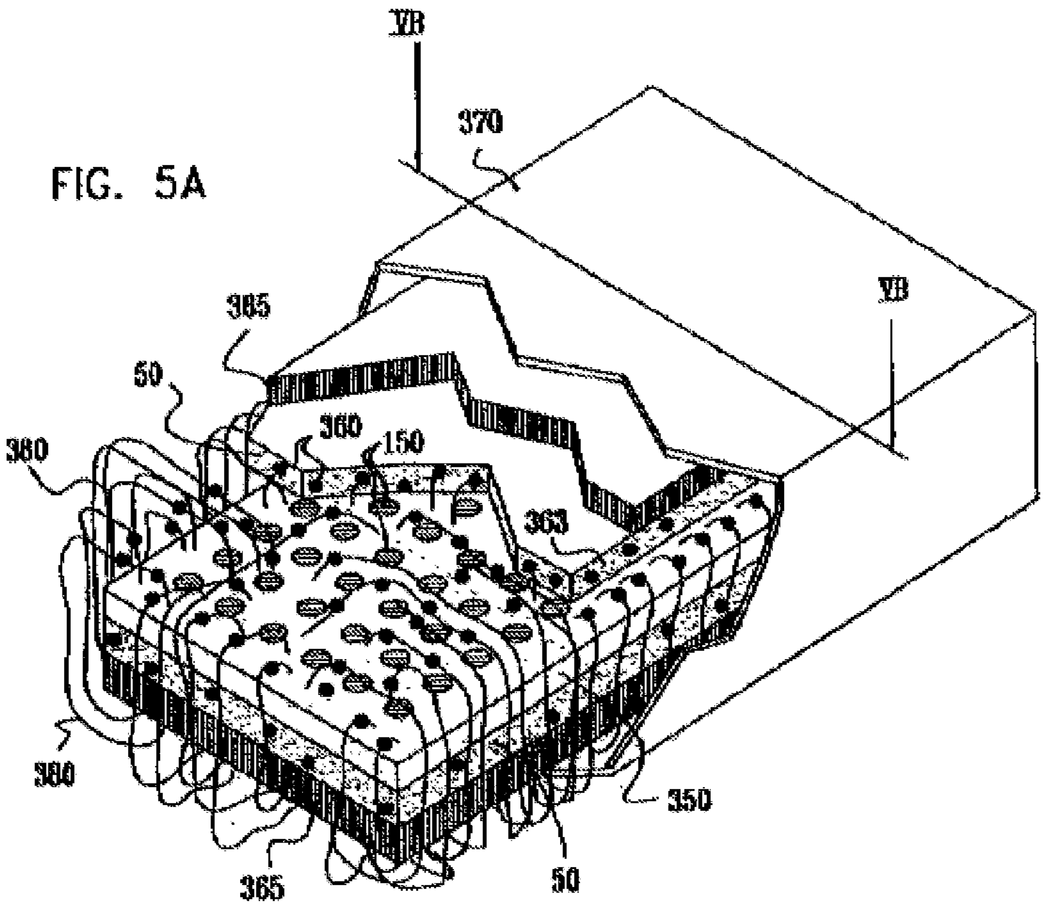

Fig. 5A of Kommerling

FIG. 1A

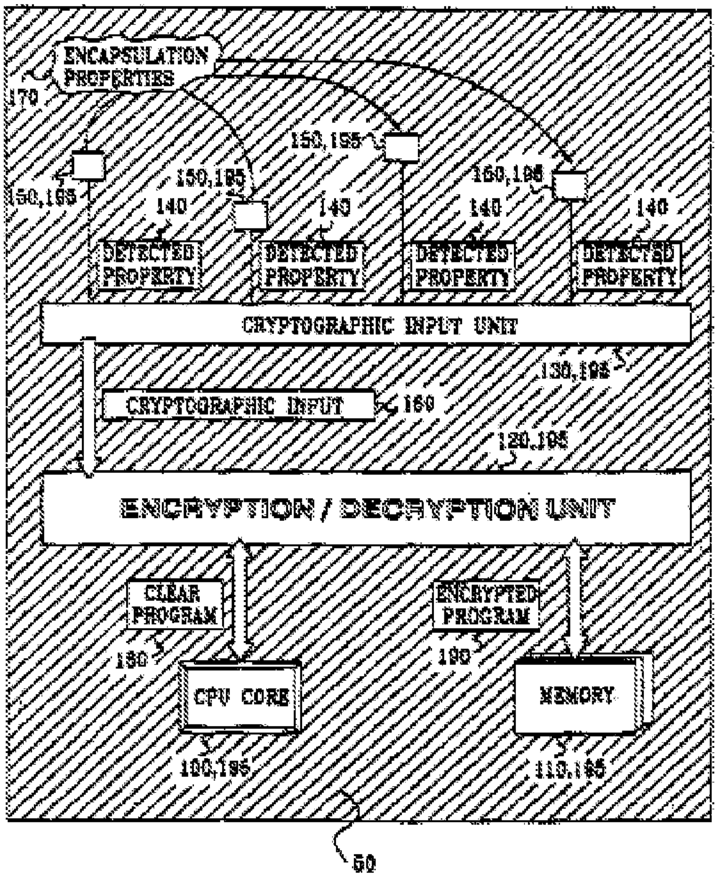

Fig. 1A of Kommerling

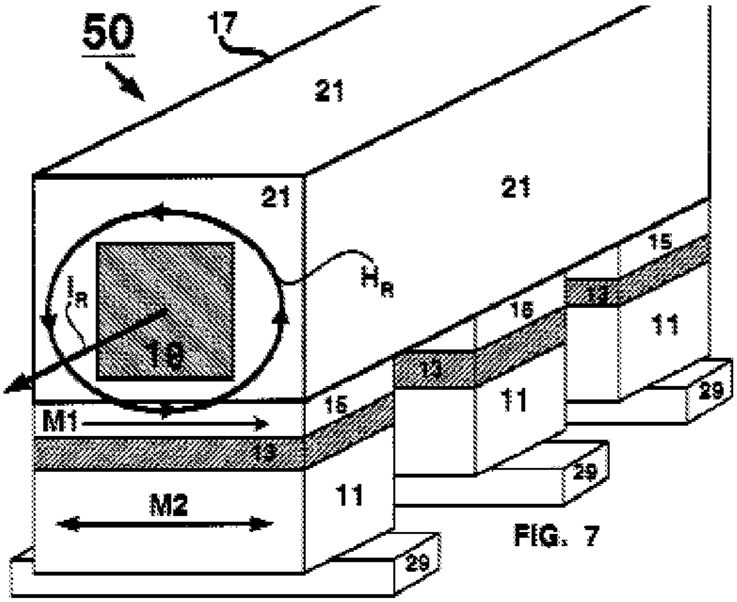

Fig. 7 of Anthony

5. Regarding claim 2, Kommerling teach that the integrated circuit arrangement of claim 1, wherein integrated circuit package and the magnetic device are arranged to direct the local magnetic field away from the plurality of mini magnets. Note in fig. 5A that the magnetic field is contained within the intact outer casing 370 away from the memory110 in fig. 1A.

6. Regarding claim 3, Kommerling teach that the integrated circuit arrangement of claim 2, wherein the magnetic device is adapted to exhibit a flinging magnetic field in response to a portion of the magnetic device being removed, the at least one of the plurality of mini magnets being exposed to the fringing field. Note in paragraphs [0114] and [0116], Kommerling teach that upon removing the outer casing 370, the distribution of the magnetic field would be changed. Due to the proximity of memory 110 to sensors 150, where the magnetic device (element 365 in fig. 5A) is located, one of ordinary skill would have recognize that memory 110 would be exposed to the strayed fringing

magnetic field upon removal of outer casing 370. Also, in the same field of endeavor, IBM teaches erasing sensitive information using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the magnetic field generated by the magnetic device (element 365) of Kommerling to exhibit a fringing magnetic field in response to a portion of the magnetic device being removed, and the storage device being exposed to the fringing field for the benefit of providing a tamper-proof storage medium.

7. Regarding claim 4, Kommerling teach that the integrated circuit arrangement of claim 1, wherein a portion of the local magnetic field of the magnetic device is aligned to an easy axis of the mini magnets. Note in paragraph [0113], Kommerling teach that the magnetic field is aligned in a convenient direction, which is perpendicular to the plates 365 in fig. 5A.

8. Regarding claim 5, Kommerling teach that the integrated circuit arrangement of claim 4, wherein the integrated circuit package includes a magnetic shield (outer casing 370 in fig. 5A) arrangement around the integrated circuit, and wherein the magnetic shield arrangement includes the magnetic device.

9. Regarding claim 6, Kommerling teach that the integrated circuit arrangement of claim 5, wherein the integrated circuit has opposite-facing top and bottom sides, and wherein the magnetic device is located adjacent the bottom side and the mini magnets are located in the top side. Note in fig. 1A, the encapsulant 50 encapsulates all

elements in fig. 1A. Furthermore, in fig. 5A, Kommerling show that a magnetic device 365 is located adjacent the bottom side of encapsulant 50.

10. Regarding claim 7, Kommerling teach that the integrated circuit arrangement of claim 6, wherein a fringing magnetic field from the magnetic device fringes out from the magnetic path in response to a portion of the magnetic device being removed. Note in paragraphs [0114] and [0116], Kommerling teach that the distribution of the magnetic field change upon removal of outer casing 370. Note that in order to remove the magnetic device 365, outer casing 370 must be removed first.

11. Regarding claim 8, Kommerling teach that the integrated circuit arrangement of claim 2, wherein the secure memory is erased upon detection of changes in the local magnetic field (paragraph [0026]). Note that erasing the secure content in a magnetic memory changes the magnetic state of the magnetic memory. Also, in the same field of endeavor, IBM teaches erasing sensitive information (thus changing the magnetic state of the storage medium by a local magnetic field from a magnetic device (current passing through a wire)) using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218).

12. Regarding claim 9, Kommerling teach that the integrated circuit arrangement of claim 2, wherein the at least one of the plurality of mini magnets changes polarity in response to the local magnetic field from the magnetic device. Note that erasing the secure content in a magnetic memory changes the polarity of the magnetic memory (paragraph [0026]). Also, in the same field of endeavor, IBM teaches erasing sensitive

information (thus changing the polarity of the storage medium by a local magnetic field from a magnetic device (current passing through a wire)) using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218).

13. Regarding claim 10, Kommerling do not teach the integrated circuit arrangement of claim 1, further comprising a sensing circuit adapted for resistively responding to a change in the magnetic state of the at least one of a plurality of mini magnets. In the same field of endeavor, Anthony teach a sensing circuit adapted for resistively responding to a change in the magnetic state of the at least one of the mini magnets (column 1, lines 66-67, column 2, lines 1-8).

14. Regarding claim 11, Kommerling do not teach the integrated circuit arrangement of claim 10, wherein the sensing circuit exhibits a first resistance in response to the at least one of the mini magnets being in a first state and exhibits a second resistance in response to the at least one of the mini magnets being in a second state. In the same field of endeavor, Anthony teach the sensing circuit exhibits a first resistance in response to the at least one of the mini magnets being in a first state and exhibits a second resistance in response to the at least one of the mini magnets being in a second state (column 1, lines 66-67, column 2, lines 1-8).

15. Regarding claim 13, Kommering do not teach the integrated circuit arrangement of claim 1, wherein the data-storage arrangement is adapted to store a bit as a function of each of the plurality of mini magnets, the bit having a value that is directly related to

the magnetic state of the mini magnets and, in response to the local magnetic field, the bit taking on a value of a magnetic state that is responsive to the local magnetic field. In the same field of endeavor, Anthony teach a data-storage arrangement is adapted to store a bit as a function of each of the plurality of mini magnets, the bit having a value that is directly related to the magnetic state of the mini magnets and, in response to the local magnetic field, the bit taking on a value of a magnetic state that is responsive to the local magnetic field (column 1, lines 41-49).

16. Regarding claim 14, Kommerling teach that the integrated circuit arrangement of claim 1, wherein at least a portion of the magnetic device (magnet 365 in fig. 5A) is outside the integrated circuit package (encapsulant 50 in fig. 5A).

17. Regarding claim 15, Kommerling teach that the integrated circuit arrangement of claim 1, wherein the integrated circuit package includes a magnetic shield (outer casing 370 in fig. 5A), the integrated circuit package is in relatively close proximity to, and surrounds, both the magnetic device and the data storage arrangement, and wherein the magnetic device is relatively distal to the data storage arrangement. Note that the magnetic device (magnet 365) is further from the data storage arrangement (memory 110 in fig. 1A) encapsulated in encapsulant 50 (the integrated circuit package) than from the ecapsulant itself (see fig. 1A and fig. 5A).

18. Regarding claim 16, Kommerling do not teach that the integrated circuit arrangement of claim 1, further comprising a write circuit adapted to write a logic state to at least one of the plurality of mini magnets by magnetizing the at least one mini magnet, the logic state being susceptible to being changed in response to the local

magnetic field. In the same field of endeavor, Anthony teach a write circuit adapted to write a logic state to at least one of the plurality of mini magnets by magnetizing the at least one mini magnet, the logic state being susceptible to being changed in response to the local magnetic field (column 2, lines 8-11).

19. Regarding claim 17, Kommerling do not teach that the integrated circuit arrangement of claim 16, wherein the write circuitry is adapted to write a first logic state to the at least one mini magnet by magnetizing the mini magnet in a first direction, and to write a second logic state to the at least one mini magnet by magnetizing the mini magnet in a second direction. In the same field of endeavor, Anthony teach the write circuitry is adapted to write a first logic state to the at least one mini magnet by magnetizing the mini magnet in a first direction, and to write a second logic state to the at least one mini magnet by magnetizing the mini magnet in a second direction (column 1, lines 41-49, column 2, lines 8-11).

20. Regarding claim 18, Kommerling teach that the integrated circuit arrangement of claim 1, wherein the magnetic device is adapted to generate a local magnetic field that sets a logic state of at least one of the mini magnets in response to a portion of the integrated circuit package being removed. Note that erasing the secure content in a magnetic memory sets a logic state of at least one of the mini magnets (paragraph [0026]).

21. Regarding claim 19, Kommerling do not teach that the integrated circuit arrangement of claim 18, wherein the magnetic device is adapted to generate a local magnetic field that sets the logic state of at least one of the mini magnets to a first logic

state. In the same field of endeavor, IBM teaches erasing sensitive information using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to adapt the magnetic device to generate a local magnetic field that sets the logic state of at least one of the mini magnets to a first logic state.

22. Regarding claim 20, Kommerling do not teach that the integrated circuit arrangement of claim 17, wherein the magnetic device is adapted to generate a local magnetic field that switches the logic state of the at least one of the mini magnets from a second logic state to the first logic state. In the same field of endeavor, IBM teaches erasing sensitive information using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention adapt the magnetic device to generate a local magnetic field that switches the logic state of the at least one of the mini magnets from a second logic state to the first logic state (erasing the information).

23. Regarding claim 21, Kommerling teach that an integrated circuit memory arrangement adapted to store data that is susceptible to data corruption (secure content erasure, paragraph [0026]) caused by a local magnetic field, the integrated circuit arrangement comprising: a plurality of sensing circuits, each sensing circuit exhibiting

an electrical characteristic that is a function of the magnetic state of at least one of the mini magnets, the electrical characteristic being detectable for reading the logical state stored in the at least one of the mini magnets (column 1, lines 66-67 and column 2, lines 1-8), an integrated circuit package (encapsulant 50 in fig. 1A) including a magnetic device (magnet 365 in fig. 5A) adapted to generate the local magnetic field, in response to the removal of a portion of the integrated circuit package, so that the magnetic state of the element storing the sensitive is altered (the secure content being erased, paragraph [0026]). However, Kommerling do not teach that the integrated circuit memory arrangement includes a plurality of mini magnets adapted to store a logical state as a function of the magnetic state of the mini magnet; a plurality of word lines, each mini magnet being magnetically responsive to a signal applied to a word line for setting a magnetic state of the mini magnet. Also, Kommerling do not teach that the local magnetic field with sufficiently strong fringe fields that the local magnetic field sets the magnetic state of the storage element storing the sensitive data. In the same field of endeavor, Anthony teach that a plurality of mini magnets adapted to store a logical state as a function of the magnetic state of the mini magnet (fig. 7, magnetic memory elements 11); a plurality of word lines, each mini magnet being magnetically responsive to a signal applied to a word line for setting a magnetic state of the mini magnet (column 1, lines 41-49 and lines 66-67, column 2, lines 1-13). Furthermore, Minakata teach that a magnetic memory can be made highly integrated (paragraph [0044]), and therefore a small magnetic memory circuit can be achieved. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a plurality of mini

magnets adapted to store a logical state as a function of the magnetic state of the mini magnet; a plurality of word lines, each mini magnet being magnetically responsive to a signal applied to a word line for setting a magnetic state of the mini magnet for the benefit that a magnetic memory can be made highly integrated, and therefore a small magnetic memory circuit can be achieved. Also, in the same field of endeavor, IBM teaches erasing sensitive information using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the magnetic field generated by the magnetic device (element 365) of Kommerling sufficiently strong fringe fields that, in response to the removal of a portion of the integrated circuit package, the local magnetic field sets the magnetic state of at least one of the mini magnets for the benefit of providing a tamper-proof storage medium.

24. Regarding claim 22, Kommerling teach that an anti-tamper arrangement adapted to protect a circuit node (memory 110 in fig. 1A), the anti-tamper arrangement comprising: magnetic means (magnet 365 in fig. 5A) for generating a local magnetic field and for directing the local magnetic field away from the circuit node; and the magnetic means further being adapted, in response to a portion of the magnetic means being removed, to sign an element in the device to cause the circuit node to take on a state (the content of the circuit node being erased, paragraph [0026]). However, Kommerling do not teach that the circuit node is a magnetically-responsive circuit node nor do Kommerling teach that the magnetic means being adapted for generating a

fringing magnetic field that causes the circuit node to take on a state. In the same field of endeavor, Anthony teach that a circuit node being magnetically responsive (element 11 in fig. 7). Furthermore, Minakata teach that magnetically responsive circuit node has the benefit of achieving a highly integrated circuit and thus a small circuit (paragraph [044]). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the circuit node magnetically-responsive circuit node for the benefit of achieving a highly integrated circuit and thus a small circuit. Also, in the same field of endeavor, IBM teaches erasing sensitive information using a magnetic field generated by a wire near a data storage device (a diskette) upon detecting of tampering attempt for the benefit of providing a tamper-proof storage medium (bottom of page 218). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to adapt the magnetic means, in response to a portion of the magnetic means being removed, for generating a fringing magnetic field that causes the circuit node to take on a state for the benefit of providing a tamper-proof storage medium.

25. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kommerling et al (PG Pub 2001/0033012 A1), in view of Anthony et al (US Patent 6,404,674 B1), further in view of Minakata et al (PG Pub 2001/0005011 A1) as applied to claim 11 above, and still further in view of Matsumoto et al (US Patent 6,194,888 B1).

26. Regarding claim 12, the previous combination remains as applied in claim 11. Furthermore, the previous combination also teaches that (column 1, lines 66-67, column 2, lines 1-13) the first and second resistances in response to the at least one of the mini magnets being in first and second states, respectively. However, the previous

combination does not teach the sensing circuit includes a transistor having a channel region exhibiting a conductance. In the same field of endeavor, Matsumoto teach that a sensing circuit includes a transistor having a conductance (column 4, lines 33-38) for the benefit of accurate conversion of impedance into a voltage (column 2, lines 16-23). Note that when an accurate conversion between impedance to voltage is achieved, the logic state of the magnetic memory can be determined. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a sensing circuit including a transistor having a channel region exhibiting a conductance for the benefit of accurate conversion of impedance into a voltage.

Response to Arguments

Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

FYL
/Feifei Yeung-Lopez/
Examiner, Art Unit 2826